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42840	7590	12/19/2005	EXAMINER	
DAVID LOWELL GARDENER 9812 HANNUM DRIVE LOS ANGELES, CA 90034			FLOURNOY, HORACE L	
			ART UNIT	PAPER NUMBER
			2189	
DATE MAILED: 12/19/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/733,953

Applicant(s)

ARIMILLI ET AL.

Examiner

Horace L. Flournoy

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 December 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

The instant application having Application No. **10/733,953** has a total of 18 claims pending in the application; there are 3 independent claims and 15 dependent claims, all of which are ready for examination by the examiner.

## INFORMATION CONCERNING OATH/DECLARATION

### *Oath/Declaration*

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

## REJECTIONS NOT BASED ON PRIOR ART

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 5-6, 9, and 12-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Because of the use of the "means for" the applicant invokes these claim to be interpreted under 35 U.S.C. 112, sixth paragraph. Accordingly, the examiner has looked to the applicant's specification to

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properly interpret these claims. It is unclear to the examiner exactly where in the specification particularly describes the structure that corresponds to the means recited in the claims.

## REJECTIONS BASED ON PRIOR ART

### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Claims 1-18** are rejected under 35 U.S.C. 102(e) as being anticipated by **Gharachorloo et al. (U.S. Patent No. 6,697,919 hereafter referred to as Gharachorloo).**

With respect to independent claim 1,

*"A data processing system, [See FIG. 1] comprising: one or more processing cores; [Gharachorloo discloses in column 4, lines 57-58, "...has eight processor cores"] and a memory controller, [Gharachorloo discloses in column 4, line 49, "...memory controller". See FIG. 1] coupled to said one or*

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*more processing cores, [Gharachorloo teaches, in column 4, lines 63-column 5, line 23, that each processor core has a memory controller. See also FIG. 1, element 118] that controls access to a system memory, [Gharachorloo discloses in column 5, lines 4-7, "Memory controller (MC) 118 that preferably interfaces directly to a memory bank of DRAM (dynamic random access memory) chips...in a memory subsystem 123."]* said memory controller having a memory speculation mechanism that stores historical information regarding prior memory accesses, [*"...and a directory..."* Also see **FIG. 4]** wherein said memory controller includes..."

The following limitations of **claim 1** are interpreted under 35 U.S.C. 112, 6<sup>th</sup> paragraph.

The Court of Appeals for the Federal Circuit, in its en banc decision *In re Donaldson Co.*, 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), decided that a "means-or-step-plus-function" limitation should be interpreted in a manner different than patent examining practice had previously dictated. The Donaldson decision affects only the manner in which the scope of a "means or step plus function" limitation in accordance with 35 U.S.C. 112, sixth paragraph, is interpreted during examination. Donaldson does not directly affect the manner in which any other section of the patent statutes is interpreted or applied.

When making a determination of patentability under 35 U.S.C. 102 or 103, past practice was to interpret a "means or step plus function" limitation by giving it the "broadest reasonable interpretation." Under the PTO's long-standing practice this meant interpreting such a limitation as reading on any prior art means or step which performed the function specified in the claim without regard for whether the prior art means or step was equivalent to the corresponding structure, material or acts described in the specification. However, in Donaldson, the Federal Circuit stated:

Per our holding, the "broadest reasonable interpretation" that an examiner may give means-plus-function language is that statutorily mandated in paragraph six. Accordingly, the PTO may not disregard the structure disclosed in the specification corresponding to such language when rendering a patentability determination. (MPEP 2181)

According to the applicant's specification in paragraph [0038], the Examiner notes that the means or system/structure ("IMC 18") for practice of the invention disclosed in the following limitation of Claim 1, is further taught in **Gharachorloo as follows:**

*“...means, responsive to a memory access request, [See FIG. 1, element 102] for speculatively [See FIGs. 4, 5, 7C, and 10C. Gharachorloo column 7, paragraphs 1-2] initiating access to the system memory [column 11, line 19, “to advance memory transactions”] based upon said historical information in said memory speculation mechanism [column 8, lines 60-63, “...the directory entry is used by the home protocol engine (HPE) 122 to maintain cache coherence of the memory lines 184 corresponding to the directory entries 182.”] in advance of receipt of a coherency message [column 21, line 64, “protocol message”] indicating that said memory access request is to be serviced by reference to said system memory.” [Gharachorloo teaches this limitation in column 22, paragraphs 1-2. Also see FIGs. 11A-14B]*

With respect to claim 2,

*“The data processing system of claim 1, wherein said memory controller and said one or more processing cores are integrated within a same integrated circuit chip.” [Gharachorloo discloses in column 2, lines 10-14, “...the Alpha 21364 aggressively exploits semiconductor technology trends by including a scaled 1 GHz 21264 core, two levels of caches, memory controller, coherence hardware, and network router all on a single die...” See FIG. 1]*

With respect to claims 3, 10 and 15,

*“The data processing system of claim 1, wherein said memory speculation mechanism comprises a memory speculation table [“directory”, See rejection*

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of claim 1 and FIGs. 4 and 10c] that stores a respective memory access history [“Directory Entry” of FIG. 4] for each of a plurality of threads executing within said one or more processing cores.” [“simultaneous multithreading (SMT)” is disclosed in column 2, line 29. Gharachorloo also discloses column 1, lines 33-34, “instruction-level parallelism and speculative out-of-order execution” which teach this limitation.]

With respect to claims 4, 11 and 16,

“The data processing system of claim 1, wherein said system memory [FIG. 1, element 123] includes a plurality of storage locations [“memory line”, abstract] arranged in a plurality of banks, [Gharachorloo discloses in column 5, lines 1-8 “each memory bank”] and wherein said memory speculation mechanism [“directory”, abstract] stores said historical information on a per-bank basis.” [Column 11, lines 56-61: “...the memory line address identifies the node 102, 104 that interfaces with the memory subsystem 123 that stores the memory line of information 184 (i.e., home node) and a specific position within the memory subsystem 123 of the memory line information.” Also see FIG. 4, elements 180, 182, 184, 123]

With respect to claims 5, 12 and 17,

The following limitations of claim 1 are interpreted under 35 U.S.C. 112, 6<sup>th</sup> paragraph.

According to the applicant's specification in paragraph [0044], the Examiner notes that the means or system/structure (“IMC 18”) for practice of the invention

disclosed in the following limitations of Claim 5 and 12, are further taught in

**Gharachorloo as follows:**

*"The data processing system of claim 1, wherein said means for speculatively initiating access [See FIG. 1, element 102] comprises means for speculatively initiating access [See FIGs. 4, 5, 7C, and 10C. Gharachorloo column 7, paragraphs 1-2] in advance of a combined response [column 11, line 19, "to advance memory transactions"] for said memory access request."*  
**[Gharachorloo teaches this limitation in column 22, paragraphs 1-2. Also see FIGs. 11A-14B]**

With respect to **claim 6**,

*"The data processing system of claim 1, wherein: said system memory comprises a first system memory; [Gharachorloo discloses this limitation in column 4, lines 63-67 – column 5, lines 1-8, "memory bank"] said memory controller comprises a first memory controller; [Gharachorloo discloses this limitation in column 4, lines 63-67 – column 5, lines 1-8, "memory controller"] said data processing system further comprising a second system memory and a second memory controller that controls access to the second system memory; [Gharachorloo teaches in column 4, lines 63-67 – column 5, lines 1-8, that each (1<sup>st</sup>, 2<sup>nd</sup>, etc...) processor core has its own memory (L1 cache, L2 cache, memory bank of DRAM) as well as memory controller. See FIGs. 1 and 2]*

*said means for speculatively initiating access comprises means for speculatively initiating access to said first system memory based upon historical information*



*recorded by said second memory controller.” [Gharachorloo discloses in column 21, lines 59-63, “The present invention includes a cache coherence protocol (CCP) that enables the sharing of memory lines of information 184 across multiple nodes 102, 104.” Gharachorloo teaches that memory speculation can be accessed by another node (processor core, memory controller, etc.: element 102 of FIG. 1) through CCP. Also see limitation in rejection of claim 1 (also interpreted under 35 U.S.C. 112 6<sup>th</sup> paragraph) With respect to the limitation, “based upon historical information recorded by said second memory controller”, the examiner notes that a second memory controller can be any of a plurality of memory controllers and therefore is interpreted as analogous to claim 1.]*

With respect to **claim 7**,

*“The data processing system of claim 1, and further comprising: a system interconnect coupling said plurality of processing cores; [See FIGs. 1-3, element 112, “Intra-chip switch (ICS)”] and one or more cache hierarchies coupled to said plurality of processing cores that cache data from said system memory.” [Gharachorloo discloses in column 4, lines 63-67, “Each processor core (PC) 106 is directly connected to dedicated instruction cache (iL1) 108 and data cache (dL1) 110 modules. These first-level caches (L1 cache modules) 108, 110 interface to other modules through an intra-chip switch (ICS) 112.”]*

With respect to **claim 8**,

*"The data processing system of claim 1, and further comprising response logic that provides said combined response for said memory access request." [FIGs. 10C-14B]*

With respect to independent **claims 9 and 14,**

*"A memory controller [Gharachorloo discloses in column 4, line 49, "...memory controller"] for controlling access to a system memory ["Memory Subsystem" FIG. 1, element 123] of a data processing system, [See FIG. 1] said memory controller comprising: a memory speculation mechanism ["directory", See FIGs. 4 and 10c] that stores historical information regarding prior memory accesses to said system memory; ["Directory Entry" of FIG. 4] and..."*

According to the applicant's specification in paragraph [0038], the Examiner notes that the means or system/structure ("IMC 18") for practice of the invention disclosed in the following limitation of Claim 9, is further taught in **Gharachorloo as follows:**

*"...means, responsive to a memory access request, [See FIG. 1, element 102] for speculatively [See FIGs. 4, 5, 7C, and 10C. Gharachorloo column 7, paragraphs 1-2] initiating access to the system memory [column 11, line 19, "to advance memory transactions"] based upon said historical information in said memory speculation mechanism [column 8, lines 60-63, "...the directory entry is used by the home protocol engine (HPE) 122 to maintain cache coherence of the memory lines 184 corresponding to the directory entries*

**182.”] in advance of receipt of a coherency message [column 21, line 64, “protocol message”] indicating that said memory access request is to be serviced by reference to said system memory.” [Gharachorloo teaches this limitation in column 22, paragraphs 1-2. Also see FIGs. 11A-14B]**

**With respect to claims 13 and 18,**

*“The memory controller of claim 9, wherein said means for speculatively initiating access comprises means for speculatively initiating access to said system memory based upon historical information recorded by another memory controller.” [Gharachorloo discloses in column 21, lines 59-63, “The present invention includes a cache coherence protocol (CCP) that enables the sharing of memory lines of information 184 across multiple nodes 102, 104.” Gharachorloo teaches that memory speculation can be accessed by another node (processor core, memory controller, etc.: element 102 of FIG. 1) through CCP. Also see limitation in rejection of claim 1 (also interpreted under 35 U.S.C. 112 6<sup>th</sup> paragraph) With respect to the limitation, “based upon historical information recorded by another memory controller”, the examiner notes that another memory controller can be any of a plurality of memory controllers and therefore is interpreted as analogous to claim 1.]*

## **CONCLUSION**

**Status of Claims in the Application**

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

**Claims rejected in the Application**

Per the instant office action, claims **1-18** have received a first action on the merits and are subject of a first action non-final.

**Direction of Future Correspondences**

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

**Important Note**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Sparks can be reached on (571) 272-4201. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more

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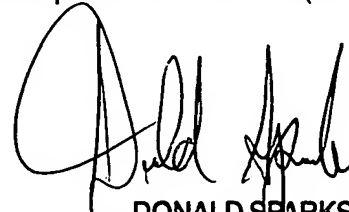
information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Horace L. Flournoy

Patent Examiner

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DONALD SPARKS  
SUPERVISORY PATENT EXAMINER